

PATENTS
Attorney Docket No. 174/188

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PATENT APPLICATION

Applicants : Andy L. Lee et al.
Filed : Herewith
For : SHIFT REGISTER IMPLEMENTATIONS OF
FIRST-IN/FIRST-OUT MEMORIES

New York, New York 10020
January 16, 2001

Hon. Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examining the above-identified,
concurrently filed patent application, please amend the
application as follows:

In the Claims

Replace claim 19 with the following amended
version of claim 19:

19. (Amended) First-in/first-out memory circuitry
comprising:

write counter circuitry configured to count,
in a Gray code, half cycles of a write clock signal that is
synchronized with successive write data words;

read counter circuitry configured to count,
in double increments of the Gray code, a read clock signal;

first shift register circuitry configured to
shift in Gray code count data produced by the write counter
and to output a Gray code count selected based on double-
increment count data produced by the read counter circuitry;
and

second shift register circuitry configured to
shift in write data words in synchronism with the write

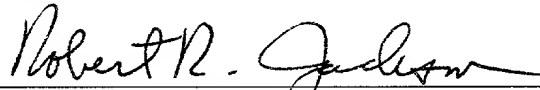
clock signal and to output a write data word selected based on the Gray code count output by the first shift register circuitry.

Remarks

Claim 19 has been amended to add several lines at the end that were inadvertently omitted when the application was put in final form. (The annexed Appendix shows the change that has been made.) Claims 1-18 and 20-35 are also in the case.

Entry of this Preliminary Amendment and favorable action on this patent application are respectfully requested.

Respectfully submitted,



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APPENDIX

(SHOWS CHANGE MADE TO CLAIM 19 IN
ACCOMPANYING PRELIMINARY AMENDMENT)

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17. A printed circuit board on which is mounted memory circuitry as defined in claim 1.

18. The printed circuitry board defined in claim 17 on which is further mounted processor circuitry coupled to the memory circuitry.

(Amended)

19. [^] First-in/first-out memory circuitry comprising:

write counter circuitry configured to count, in a Gray code, half cycles of a write clock signal that is synchronized with successive write data words;

read counter circuitry configured to count, in double increments of the Gray code, a read clock signal;

first shift register circuitry configured to shift in Gray code count data produced by the write counter and to output a Gray code count selected based on double-increment count data produced by the read counter circuitry; and

20. The memory circuitry defined in claim 19 further comprising:

detector circuitry configured to compare the Gray code count output by the first shift register circuitry to a predetermined count indicative of a particular capacity condition of the second shift register circuitry.

21. The memory circuitry defined in claim 20 wherein the capacity condition is an empty condition.

21. The memory circuitry defined in claim 20 wherein the capacity condition is an empty condition. A second shift register circuitry configured to shift in write data words in synchronism with the write clock signal and to output a write data word selected based on the Gray code count output by the first shift register circuitry.